Product List

OB38A08T1W16,
OB38A08T1W14,
OB38A08T1W10,

Description

The OB38A08T1 is a 1T (one machine cycle per clock) single-chip 8-bit microcontroller. It has 8KB embedded program memory, and executes all ASM51 instructions fully compatible with MCS-51.

OB38A08T1 contains 512B on-chip RAM, up to 14 GPIOs (16L package), various serial interfaces and many peripheral functions as described below. It can be programmed via writers. Its on-chip ICE is convenient for users in verification during development stage.

The high performance of OB38A08T1 can achieve complicated manipulation within short time. About one third of the instructions are pure 1T, and the average speed is 8 times of traditional 8051, the fastest one among all the 1T 51-series. Its excellent EMI and ESD characteristics are advantageous for many different applications.

Ordering Information

OB38A08T1 ihhkL
YWW
i： process identifier { W = 2.4V ~ 5.5V}
hh：pin count
k：package type postfix {as table below }
L：PB Free identifier
{No text is Non-PB free，”P” is PB free}
Y：Year Code
WW：Week Code (01-52)

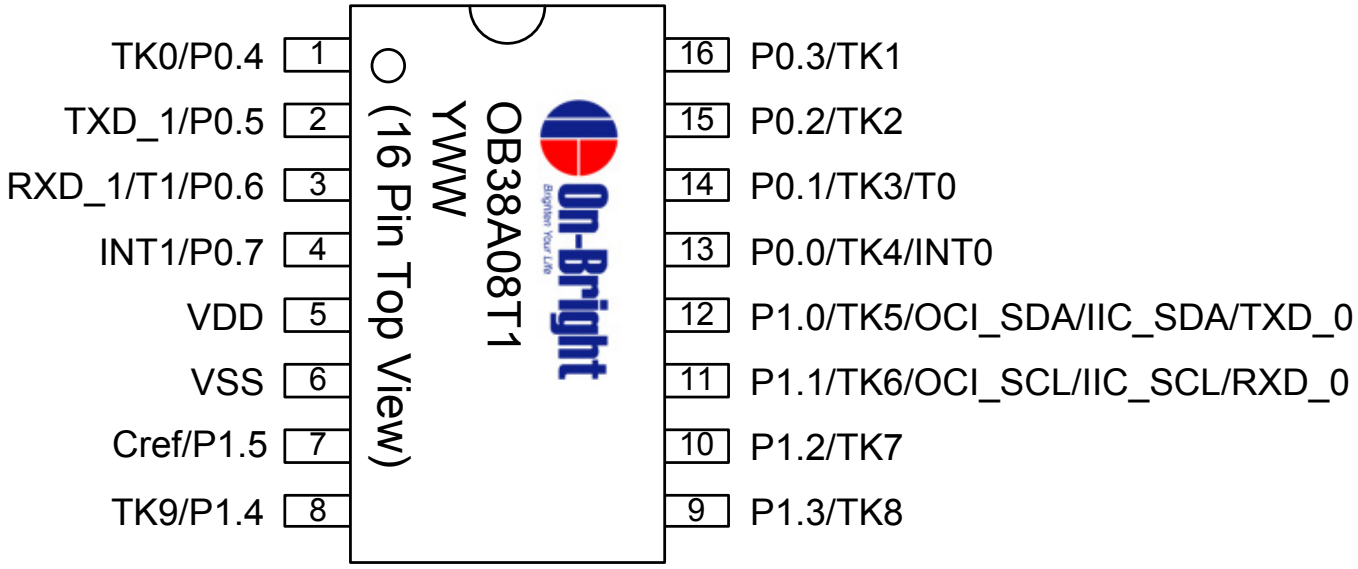
Postfix	Package
O	SOP (150 mil)
G	SSOP (150 mil)
M	MSOP (118 mil)

Features

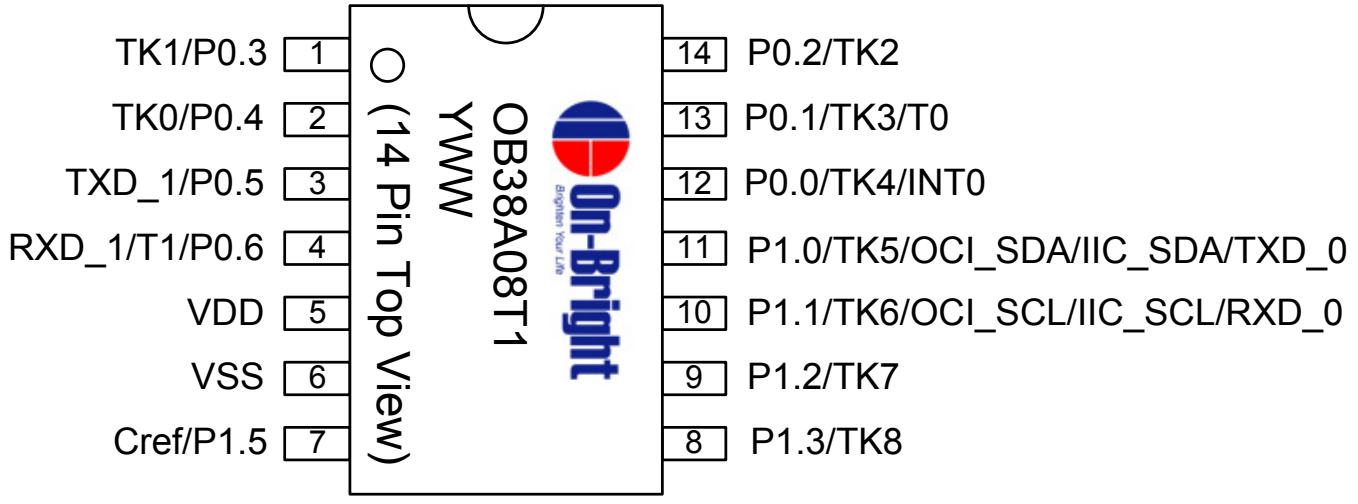
- Operating Voltage: 2.4V ~ 5.5V
- High speed architecture of 1 clock/machine cycle runs up to 16MHz.
- 1~8T can be switched on the fly.
- Instruction-set compatible with MCS-51.
- 16MHz Internal RC oscillator, with programmable clock divider
- 8KB on-chip program memory.
- 256 bytes SRAM as standard 8052, plus 256 bytes on-chip expandable SRAM.
- Dual 16-bit Data Pointers (DPTR0 & DPTR1).
- One serial peripheral interfaces in full duplex mode.
- Up to 10 touch sense inputs, support multiplexing I/O function.
- Lower power touch-key wakeup function.
- Additional Baud Rate Generator for Serial port.
- Two 16-bit Timer/Counters. (Timer 0,1）
- Port 0~1, Up to 14 GPIO.
- External interrupt 0,1 with four priority levels
- Programmable watchdog reset and interrupt timer.
- One IIC interface. (Master/Slave mode)
- ISP/IAP/ICP functions.
- ISP service program space configurable in N*128 byte (N=0 to 8) size.
- EEPROM function.
- On-Chip in-circuit emulator (ICE) functions with On-Chip Debugger (OCD).
- LVI/LVR (LVR deglitch 500ns)
  - POR and Programmable LVR(3.0 / 2.4 / 2.2 /2.0) & LVI (4.0 / 3.2 / 2.6 / 2.4)
- 2 external interrupt with rising/falling edge detection. (INT x 2)
- Power management unit for IDLE and power down modes.

Pin Configuration

16 Pin SOP 150mil



14 Pin SOP 150mil



10 Pin MSOP 118mil